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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/614,628	07/03/2003	Andrew Dunshea	AUS920030164US1	7847
7590	08/22/2005		EXAMINER	
Marilyn Smith Dawkins Intellectual Property Law Dept. IBM Corporation 11400 Burnet Road Austin, TX 78758			WALTER, CRAIG E	
			ART UNIT	PAPER NUMBER
			2188	
DATE MAILED: 08/22/2005				

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/614,628	DUNSHEA ET AL.	
	Examiner	Art Unit	
	Craig E. Walter	2188	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --
Period for Reply

**A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM
 THE MAILING DATE OF THIS COMMUNICATION.**

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

- 1) Responsive to communication(s) filed on 03 July 2003.
- 2a) This action is FINAL. 2b) This action is non-final.
- 3) Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

- 4) Claim(s) 1-20 is/are pending in the application.
- 4a) Of the above claim(s) _____ is/are withdrawn from consideration.
- 5) Claim(s) 16-20 is/are allowed.
- 6) Claim(s) 1,5 and 7-15 is/are rejected.
- 7) Claim(s) 2-4 and 6 is/are objected to.
- 8) Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

- 9) The specification is objected to by the Examiner.
- 10) The drawing(s) filed on 03 July 2003 is/are: a) accepted or b) objected to by the Examiner.
 Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).
 Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).
- 11) The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

- 12) Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
 - a) All b) Some * c) None of:
 1. Certified copies of the priority documents have been received.
 2. Certified copies of the priority documents have been received in Application No. _____.
 3. Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

- | | |
|---|---|
| 1) <input checked="" type="checkbox"/> Notice of References Cited (PTO-892) | 4) <input type="checkbox"/> Interview Summary (PTO-413) |
| 2) <input type="checkbox"/> Notice of Draftsperson's Patent Drawing Review (PTO-948) | Paper No(s)/Mail Date. _____ . |
| 3) <input checked="" type="checkbox"/> Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08)
Paper No(s)/Mail Date <u>7/3/03</u> . | 5) <input type="checkbox"/> Notice of Informal Patent Application (PTO-152) |
| | 6) <input type="checkbox"/> Other: _____ . |

Information Disclosure Statement

1. The information disclosure statement received on 7/3/2003 was fully considered by the examiner.

Claim Objections

2. Claims 12-15 are objected to because of the following informalities:

As for claim 12, the phrase "re-reference indicator" in lines 7-8 should be changed to "reference indicator".

Claims 13-15 directly depend on claim 12 therefore they too are objected to for the reason set forth above.

Appropriate correction is required.

Claim Rejections - 35 USC § 101

35 U.S.C. 101 reads as follows:

Whoever invents or discovers any new and useful process, machine, manufacture, or composition of matter, or any new and useful improvement thereof, may obtain a patent therefor, subject to the conditions and requirements of this title.

3. Claims 7-15 are rejected under 35 U.S.C. 101 as being not limited to tangible embodiments. In view of applicants' disclosure, specification page 7, lines 23-30, the signal-bearing medium is not limited to tangible embodiments, instead being defined as including both tangible embodiments (i.e. read only memory as described in lines 23-25) and intangible embodiments (i.e. wireless communications as described in lines 28-30).

As such, these claims are not limited to statutory subject matter and are therefore non-statutory.

Claim Rejections - 35 USC § 102

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless –

(b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

4. Claims 1 and 5 are rejected under 35 U.S.C. 102(b) as being anticipated by Arai et al. (hereinafter Arai) US Patent 5,193,172.

As for claim 1, Arai teaches a method comprising:

receiving an instruction to access a first page (the page stealing operation (which is described in greater detail in col. 6, lines 45-60) occurs in response to a page fault. The page steal unit will steal pages which the processor does not keep based on the page's use priority – col. 5, lines 47-61); and

determining whether to replace a second page in memory with the first page based on a reference indicator and a re-reference indicator for the second page (a reference bit and a UIC bit (reference and re-reference respectively) are used to determine when to steal a page – col. 6, lines 50-60), wherein the reference indicator indicates whether the second page has been accessed since the second page was loaded into the memory, and wherein the re-reference indicator indicates whether the second page has been accessed

subsequent to the reference indicator being set (the reference bit of the page is retrieved, if the bit is set (i.e. page has been accessed) the bit is cleared and the UIC bit is cleared to zero, if the reference bit is off, the UIC bit is incremented. The page will be stolen based on a comparison between the value of the UIC and a predetermined threshold – col. 6, lines 50-60).

As for claim 5, Arai teaches the method of claim 1, wherein the reference indicator is set by a memory management unit (control unit for memory management (col. 6, lines 1-6) comprises the steal unit) when the second page is accessed and the reference indicator was previously clear (page stealing will occur when the reference indicator is clear and the UIC bit is reaches it predetermined threshold (col. 6, lines 52-60)).

Allowable Subject Matter

5. Claims 2-4, 6 and 16-20 are allowable over the prior art of record.
6. Claims 7-15 are allowable over prior art of record, but are rejected under 35 U.S.C. 101 as set forth above.
7. The following is a statement of reasons for the indication of allowable subject matter:

As for claim 2, though Arai teaches all the limitations of claim 1, he fails to teach replacing the page if both indicators are clear.

As for claim 3, though Arai teaches all the limitations of claim 1, he fails to teach replacing the page if the reference indicator is set and the re-reference indicator is clear.

As for claim 4, Arai does not teach clearing both the reference and re-reference bits if both are set and all pages in memory are in use. Arai rather teaches clearing the reference indicator prior to setting the re-reference indicator.

As for claim 6, Arai fails to teach setting the re-reference indicator after reference indicator was set. Arai rather teaches clearing the re-reference indicator after the reference indicator was set.

As for claim 7, though Arai teaches storing allocated pages in a memory management table (col. 6, lines 40-45), and teaches the use of a reference and re-reference indicator, he fails to teach replacing the page if both the reference and re-reference are cleared (see reason for allowance set forth in the discussion of claim 2 above).

As for claim 12, though Arai teaches storing allocated pages in a memory management table (col. 6, lines 40-45), and teaches the use of a reference and re-reference indicator, he fails to teach setting the re-reference indicator once a page has been accessed, and the reference indicator was previously set (rather Arai teaches clearing both indicators when the page is referenced since the first reference indicator was set).

Additionally with respect to claims 7 and 12, Ezra US Patent 6,594,742 B1 discloses a system and method for cache management via statistically adjusted

slot aging. Ezra teaches a method which maintains an age table (page table) containing an age value for corresponding slots (pages) in memory (col. 2, lines 1-11). As each entry is accessed, the corresponding age value contained within the table is incremented. The age value is then compared to a preset, maturity age associated with the processor (col. 2, lines 7-14). Entries that exceed the preset maturity age of the processor are the first to be evicted from the memory (col. 2, lines 27-35). Though the age value contained in the table is functioning as a counter, used to determine the number of times a particular entry has been accessed (i.e. referenced, then re-referenced), Ezra fails to provide for evicting an entry based on the status of two distinct indicators as claimed by applicant.

As for claim 16, though Arai teaches storing allocated pages in a memory management table (col. 6, lines 40-45), and teaches the use of a reference and re-reference indicator, he fails to teach setting the re-reference indicator once a page has been accessed and the reference indicator was previously set (rather Arai teaches clearing both indicators when the page is referenced since the first reference indicator was set).

Additionally with respect to claim 16, though Ezra teaches an age table (page table) comprising a plurality of entries, wherein each of the plurality of entries has a reference indicator and a re-reference indicator (age value); and a memory management utility to set the reference indicator when an associated page is accessed in main memory (the processor will increase the age value of the entry each time it is accessed) - col. 2, lines 1-14. As discussed above for

claims 7 and 12, Ezra fails to teach evicting an entry based on the status of two distinct indicators as claimed by applicant.

As for claim 16, though Arai teaches setting a reference indicator in a page table when a page in main memory is accessed and the previous entry was clear, he fails to teach setting the re-reference indicator when the page is accessed since the reference indicator was set. Furthermore, Arai fails to teach a secondary storage device with a virtual memory manager to clear the reference and re-reference indicators.

Additionally with respect to claim 18, though Ezra's system allows for the processor to set an indicator (age value) in a page table entry when the entry is accessed, he fails to teach evicting an entry based on the status of two distinct indicators as claimed by applicant. Furthermore, Ezra fails to teach a secondary storage containing a virtual memory manager that clears both said indicators if they were previously set, the main memory is full, and a new page from the secondary storage is accessed.

Claims 8-11, 13-15, 17 and 19-20 further limit claims 7, 12, 16 and 18 respectively therefore they too are allowable over the prior art of record.

Remarks

8. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure:

Azuma (US PG Publication 2004/0181633 A) discloses a cache memory system utilizing a plurality of reference bits for each entry in the cache. Referring to Fig. 4, Azuma illustrates the use of two reference bits RA and RB for each entry in the cache (both of which are initially set to zero). RA is enabled (i.e. set to 1) at the onset of the first cache hit (step "A" as illustrated in the figure). The line has now been "referenced" – paragraph 0063, lines 10-24. Further, when a subsequent hit occurs (step "C") RB is enabled, now both bits (reference and re-reference) are enabled (step "D") – Also see paragraphs 0065 and 0066.

Though he utilizes a reference and re-reference bit as claimed by applicant's invention, Azuma fails to use the status of these bits to make a determination to replace the page. By contrast, Azuma feeds the bit information to a bit judgment circuit (Fig. 2, element 6) which is used in concert with bit information provided from other cache lines to make a determination which line to replace. Rather than relying upon a replacement procedure based on the status of two bits (reference and re-reference) as claimed by applicant, Azuma's system determines the value of the reference bit RS by considering information of entry hits by taking a logical sum of the values of the old reference bit and the current reference bit (paragraph 0075, lines 10). In an alternative embodiment, Azuma's

system can determine the value of the reference bit TS based on the number of times the entry is hit using a counter (paragraph 0075, 15-21).

Shuf et al. (hereinafter Shuf) US Patent 6,886,085 B1 disclose a method and apparatus for efficient virtual memory management. Though Shuf teaches a memory utilizes two history (reference) bits, “changed” and “reference”, the latter is enabled upon a load instruction and both are enabled upon a store instruction (col. 10, lines 27-31). Though these two bits are used to make a determination if and when a page is to be swapped, the bits are mutually exclusive, i.e. one bit does not necessarily need to be set before the second is set as claimed by applicant. In addition, Shuf discloses swapping a page out of memory when the a page is unmodified (i.e. the changed bit is not enabled) in col. 10, lines 48-53 rather than marking pages for eviction that have been re-referenced (i.e. accessed since the subsequent access to the page) as claimed by applicant.

Johnson et al. (hereinafter Johnson) US PG Publication 2003/0084253 A1 disclose an age bit associated with each cache line is reset to indicate that a particular line has been accessed (first reference indication). Each cache line is then subsequently scanned periodically to determine if the age-bit is enabled (i.e. line has been accessed since the last modification). If the bit is enabled, the bit is set to a second state (second reference indication, or re-reference indication). Determination for eviction of the cache line is then based on the status of the age-bit (i.e. a stale cache line is one in which the age-bit is set to the second state) – Paragraph 0010, lines 9-22. Johnson’s teachings therefore fail to meet

the limitations of claim 1 which stipulates setting the re-reference indicator upon an **access** to the page in cache, rather than setting the second indication by periodically **scanning** the indicator of each cache line to determine if the line is stale as taught by Johnson.

Conclusion

9. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Craig E. Walter whose telephone number is (571) 272-8154. The examiner can normally be reached on 8:30a - 5:00p M-F.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Mano Padmanabhan can be reached on (571) 272-4210. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see <http://pair-direct.uspto.gov>.

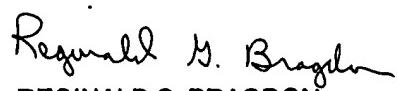
Art Unit: 2188

Should you have questions on access to the Private PAIR system, contact the
Electronic Business Center (EBC) at 866-217-9197 (toll-free).



Craig E Walter
Examiner
Art Unit 2188

CEW



REGINALD G. BRAGDON
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